REMARKS

Claims 3-7 and 9-29 were previously pending in this application. New claims 30-32 are added herein. Claims 11 and 24 are amended herein. No claims have been canceled. As a result claims 3-7 and 9-32 are pending for examination with claims 11, 15, 24 and 30 being independent claims. No new matter is added by these amendments. Support for new claims 30-32 can be found in the originally-filed figures and in the specification, for example, at page 8, lines 21-25, page 9, lines 8-12, and page 10, lines 17-22.

Summary of Telephone Conference with Examiner

Applicants thank Examiner Vent for her time and courtesy during the telephone interview conducted on February 6, 2007 with the undersigned. During the interview the parties discussed the subject matter of the cited references U.S. Patent No. 6,678,002 to Frink et al. (hereinafter "Frink"), U.S. Patent No. 6,853,385 to MacInnis et al. (hereinafter "MacInnis") and U.S. Patent No. 5,956,046 to Kehlet et al (herein after "Kehlet"). The parties also discussed a claim corresponding to new claim 30. Examiner Vent stated that further search and examination were required concerning the patentability of the claims.

Rejections Under 35 U.S.C. §103

The Office Action rejects claims 3-7 and 9-29 under 35 U.S.C. §103(a) as being unpatentable over Frink in view of MacInnis and further in view of Kehlet. Applicants respectfully disagree because none of Frink, MacInnis or Kehlet teach or suggest a graphics accelerator including at least two video inputs for receiving at least two real-time uncompressed digital video streams. Further, none of Frink, MacInnis or Kehlet teach or suggest that a graphics accelerator performs video editing of at least two real-time uncompressed digital video streams and generates an edited uncompressed digital video stream at a video output of the graphics accelerator, wherein said edited uncompressed digital video stream includes edited video from at least one of the first real-time uncompressed digital video stream and the second real-time uncompressed video stream

At page 5, the Office Action relies on Kehlet to teach "that a graphic accelerator chip can have two inputs as seen in Figure 3 and further described in Column 5 lines 45+." The Applicants respectfully assert, however, that the combination of Frink, MacInnis and Kehlet do not provide a *prima facie* case of obviousness because they do not teach or suggest all the limitations of the claims. Referring to Kehlet, the mere teaching of a graphics accelerator that supplies graphics data from a single graphics pipeline to each of two frame buffer memories does not say anything at all about a graphics accelerator chip that includes two inputs, or in particular, anything at all about a graphics accelerator chip that includes at least two video inputs for receiving at least two real-time uncompressed digital video streams, for example, as recited in claim 11. (Emphasis added.)

1. Kehlet

Kehlet does not teach or suggest a graphics accelerator chip having at least two video inputs for receiving at least two real-time uncompressed digital video streams at least because: 1) the frame buffers 202A and 202B of Kehlet receive graphics data they do not receive any real-time uncompressed digital video streams; 2) the graphics pipeline is a single source of graphics data; thus, the frame buffers do not receive at least two streams of any type of data because the frame buffers receive the graphics data from the same prior stage of the graphics pipeline, accordingly, Kehlet does not describe that a graphics accelerator includes two inputs; and 3) if for the sake of argument and in contrast to the Applicants' position Kehlet is seen as teaching two inputs, the mere teaching of two inputs to a graphics accelerator does not teach or suggest at least two video inputs for receiving at least two real-time uncompressed digital video streams.

Kehlet teaches that a frame buffer memory 0 and a frame buffer memory 1 of a graphics accelerator each "receive pixel data from previous stages of the graphics pipeline." (Col. 5, lines 45-51.) Kehlet further teaches that "[g]raphics accelerators 40A and 41A shown in FIGS. 3 and 4 implement double buffering of frame buffer memory." (Col. 8, lines 4-6.) From Wikipedia, "[d]ouble buffering" allows the "use [of] two separate buffers in parallel, so that while [a first buffer] B1 is read [a second buffer] B2 can be written, and while B2 is read B1 can be written." As taught by Kehlet, the graphics accelerator 40A employs double buffers in the general manner

described in Wikipedia. That is, the graphics accelerator is included in a graphics pipeline and includes frame buffers that alternately receive data from preceding elements in the graphics pipeline and output data for display. Each frame buffer is connected to the same graphics pipeline. Thus, while a first frame buffer is outputting a scene for display, a second frame buffer is receiving data for the subsequent scene.

Regarding item 1) above, the graphics accelerators of Kehlet receive graphics data. Kehlet does not describe that the graphics accelerators receive any real time uncompressed video streams let alone at least two real-time uncompressed digital video streams. Instead, Kehlet describes that "a single host CPU may provide graphics input data to all of graphic accelerators 40." (Col. 4, lines 60-62.)

Regarding item 2) above, Kehlet repeatedly refers to the graphics pipeline in the singular. Kehlet does not provide any teaching or suggestion that the frame buffers receive graphics data from two different graphics pipeline. For example, Kehlet refers to "previous stages in graphics pipeline" (Fig. 1), "front end of the pipeline of graphics accelerator 40 then performs geometry processing operations on the received input data, producing modified geometric primitive data" (col. 4, lines 36-39), "each graphics accelerator 40 receives geometry input data from a host CPU" (col. 4, lines 34-36), and "[m]emory banks 202 receive pixel data from previous stages of the graphics pipeline" (Co. 5, lines 49-51). (Emphasis added.) Thus, Kehlet does not teach or suggest that the graphics accelerators 40 receive data at a plurality of graphics inputs let alone that the graphics accelerators 40 receive data at two or more video inputs for receiving at least two real-time uncompressed digital video streams.

Further, Fig. 5 does not show any actual inputs to the graphics accelerators. Instead, Fig. 5 illustrates an input to the frame buffers of the graphics accelerators. Although the specification teaches that in an alternate embodiment the host CPU can provide "modified geometric primitives" to the graphics accelerators (col. 4, lines 49-54), Kehlet does not teach or suggest that the graphics accelerator is actually coupled to the CPU by more than one input.

Referring to item 3), the mere teaching of two inputs of any type by a reference applied in combination with Frink and MacInnis is not sufficient to teach or suggest all the limitations of the claims. The deficiencies of Frink and MacInnis are described below. In addition, however,

as described by inventor Andre Laframboise in the telephone interview of June 26, 2007, some embodiments of Applicants invention employ a graphics accelerator in a manner that allows the graphics accelerator to perform editing of at least two real-time uncompressed digital video streams. None of the cited references teach or suggest such a method or any apparatus to achieve such a result. The identification of a reference that teaches or suggests that a graphics accelerator can generally include two inputs does not change the preceding facts because it fails to provide a teaching or suggestion of all the limitations of the claims even when combined with Frink and MacInnis.

2. Frink and MacInnis

Neither Frink nor MacInnis cure the deficiencies of Kehlet. Applicants response of July 23, 2007 describes in detail why Frink and MacInnis either alone or in proper combination do not teach or suggest, a graphics accelerator chip that includes, at least two video inputs for receiving at least two real-time uncompressed digital video streams. The instant Office Action does not appear to rely on either Frink or MacInnis to teach or suggest a graphics accelerator chip that includes, at least two video inputs for receiving at least two real-time uncompressed digital video streams. Accordingly, Applicants summarize those remarks below rather than repeat them in-full in this Amendment and Response and do so in the interest of completeness.

Instead of describing that a graphics accelerator is employed to edit real time uncompressed digital video streams, Frink expressly indicates that video editing is performed elsewhere in a video system, namely in the HD DVE module 554 and the HDTV 3D DVE module 550. (See col. 10, lines 30-39, describing that 3D digital video effects, compositing, etc. are performed in the modules 554 and 550.)

Frink describes that a graphics accelerator 552 may combine video with graphics but indicates that video editing operations including 3D video effects are performed in the HD DVE module 554. Accordingly, Applicants respectfully assert that a close review of Fig. 5 which is fully consistent with the remainder of Frink finds that graphics and video are provided to the graphics accelerator 552 from the module 520 and that video and key are communicated from the graphics accelerator 552 back to the module 520. Accordingly, Frink also fails to teach or

suggest "a graphics accelerator chip having at least two video inputs for receiving at least two real-time uncompressed digital video streams" as recited in claims 11 and 24.

MacInnis dedicates approximately three columns to a description of the graphics accelerator 64 and its operation. (Col. 59, line 55 through col. 62, line 54.) In this substantial description, MacInnis does not provide any teaching or suggestion that the graphics accelerator 64 even receives a real time uncompressed video stream. Instead, MacInnis teaches a system in which video and graphics are processed in separate processing pipelines before being combined in a compositor 108. (See Fig. 4.) That is, MacInnis employs "a dedicated processor" that includes "a memory for graphics data including pixels, and a coprocessor for performing vector type operations on a plurality of components of one pixel of graphics data." (Col. 59, lines 60-67, emphasis added.) As further explained in col. 60, "a graphics accelerator 64 receives commands from a CPU 22 and receives graphics data from main memory 28 through a memory controller 54." (Col. 60, lines 26-28, emphasis added.) Thus, MacInnis fails to teach or suggest that any real-time uncompressed video streams are supplied to a graphics accelerator let alone that at least two real-time uncompressed digital video streams are supplied to a graphics accelerator.

3. Pending Claims

Claims 11 and 24 recite a graphics accelerator chip having at least two video inputs for receiving said at least two real-time uncompressed digital video streams. Claim 15 recites acts of receiving a first real-time uncompressed digital video stream at a first input of the graphics accelerator chip and receiving a second real-time uncompressed digital video stream at a second input of the graphics accelerator chip.

In addition, new claim 30 recites a graphics accelerator chip having a first video input configured to receive a first real-time uncompressed digital video stream including a first plurality of video frames and a second video input configured to receive a second real-time uncompressed digital video stream including a second plurality of video frames.

Further, claims 11 and 24 recite a graphics accelerator chip having a 2D graphics engine and a 3D rendering engine respectively for providing 2D and 3D functions used for said video

editing of said at least two real-time uncompressed digital video streams, said graphics accelerator chip further comprising a video output for providing edited uncompressed digital video streams. Claim 15 recites acts of generating an edited uncompressed digital video stream at a video output of the graphics accelerator chip, wherein said edited uncompressed digital video stream includes edited video from at least one of the first real-time uncompressed digital video stream and the second real-time uncompressed video stream.

In addition, new claim 30 recites a 2D graphics engine and a 3D rendering engine each coupled to the first video input, the second video input and the graphics input, the 2D graphics engine and the 3D graphics engine configured to provide 2D and 3D functions, respectively, and to perform video editing in real time of the first real-time uncompressed digital video stream and the second real-time uncompressed digital video stream to generate an edited uncompressed digital video stream that includes at least a portion of one video frame of the first plurality of video frames, at least a portion of one video frame of the second plurality of video frames and the graphics data; and a video output configured to output the edited uncompressed digital video stream

For all of the above reasons, Applicants respectfully assert that none of Frink, MacInnis or Kehlet alone or in proper combination teach or suggest all the limitations recited in independent claims 11, 15, 24 and 30. Each of claims 3-7, 9, 10, 12-14, 16-23 and 25-29 depend from one of the allowable independent claims. Accordingly, reconsideration and withdrawal of the rejections of claims 3-7 and 9-29 is respectfully requested.

Amendment to Independent Claims 11 and 24

The first occurrence of the term "respectively" is deleted from each of independent claims 11 and 24. Applicants respectfully assert that these amendments make claims 11 and 24 clearer and do not change their scope. In particular, following these amendments, each of claims 11 and 24 continue to include at least two video inputs where each video input can receive one or more real-time uncompressed digital video streams. Applicants respectfully assert that the preceding corresponds to the prior language of claims 11 and 24 but with added clarity.

CONCLUSION

In view of the foregoing amendments and remarks, reconsideration is respectfully requested. This application should now be in condition for allowance; a notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

A petition and fee for a one month extension of time is included herewith. If this response is not considered timely filed and if a request for an extension of time is otherwise absent in view of the accompanying petition and fee, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed payment, please charge any deficiency to Deposit Account No. 50/2762, M1073-700719.

Respectfully submitted,
Lorne Trottier et al., Applicants

By: /Robert V. Donahoe/
Robert V. Donahoe, Reg. No. 46,667
LOWRIE, LANDO & ANASTASI, LLP
One Main Street
Cambridge, Massachusetts 02142
United States of America
Telephone: 617-395-7000
Facsimile: 617-395-707